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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,825	07/02/2003	Robert W. Boesel	029573-0301	3912

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EXAMINER

TU, JULIA P

ART UNIT	PAPER NUMBER
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2611

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/613,825	BOESEL ET AL.	
	Examiner	Art Unit	
	Julia P. Tu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on July 2, 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-6, 30, 31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1 and 30 constitutes abstract ideas and therefore is a judicial exception and not statutory subject matter. Also the abstract ideas are not used in a practical application to provide a useful, concrete, and tangible result.

Claims 2-6 and 31 are rejected as incorporating the deficiency of claims 1 and 30 upon which they depend.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Easton et al. (US 6,985,516).

(1) with regard to claim 1:

As shown in figures 2 and 5, Easton discloses a method for demodulation of a composite signal containing a plurality of multi-path components, the method comprising:

buffering digital samples of a signal into a first memory element (block 224 in figure 5);

randomly accessing the digital samples from the first memory element to correlate a particular multi-path component from the signal (block 522 in figure 5); and

iteratively accumulating the correlated particular multi-path component into a second memory element (blocks 524, 526, and 234 in figure 5).

(2) with regard to claim 2:

Easton further teaches accessing digital samples according to paths corresponding to the digital samples (see figures 2 and 6A).

(3) with regard to claim 3:

Easton further teaches wherein iteratively accumulating the correlated particular multi-path component into a second memory element defines a demodulation operation and comprises using information from the signal to determine an amount of demodulation processing to be performed (see figures 2, 3, and 4).

(4) with regard to claim 4:

Easton further teaches the determination of multi-path components to be iteratively processed varies dynamically between processing units (see figure 2).

(5) with regard to claim 6:

As shown in figure 2, Easton further discloses tuning to a non-original RF frequency (block 214 in figure 2);

buffering digital samples obtained while tuned at the non-original RF frequency (block 224 in figure 2);

retuning the RF frequency to the original frequency (see block 214 in figure 2);
and

performing searching and channel estimation via the random access of the digital samples stored in the first memory element (see block 224 in figure 2) while simultaneously operating on the digital samples of the original frequency (see blocks 214 and 224 in figure 2).

4. Claims 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 2004/0165567).

(1) with regard to claim 30:

As shown in figures 3-7, Kim discloses a method of processing data based on programmed instructions, the method comprising: demodulating a CDMA-compliant waveform, wherein the CDMA-compliant waveform is processed asynchronously to a sample rate associated with the waveform during processing of communication chips

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and based on programmed instructions in programmed memory (see figures 3-7, page 1, paragraphs [0013]).

(2) with regard to claim 31:

Kim discloses the entire demodulation processing is done asynchronously (asynchronous CDMA, page 1, paragraph [0013]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5, 7-8, 11-12, 15-25, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton et al. (US 6,985,516) in view of Usuda et al. (US 6,853,839).

(1) with regard to claim 5:

Easton discloses all of the subject matters in claim 1 above but does not explicitly teach performing channel estimation via the non-sequential access of digital samples from the first memory element.

However, Usuda teaches performing channel estimation via the non-sequential access of digital samples (see block 303 in figure 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Usuda into the teaching of Easton in order to improve the reliability of

the antenna weight for the data demodulation as well as to improve the communication quality and increase the radio channel capacity (column 3, lines 36-38 and lines 53-54).

(2) with regard to claim 7:

As shown in figures 2 and 5, Easton discloses an apparatus configured to demodulate a composite signal containing a plurality of multi-path components, the apparatus comprising:

buffers configured to be switchable between a write state with digital samples and a read state by a correlating element (see block 224 in figure 5);

a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component (column 12, lines 24-29);

an accumulator that iteratively accumulates the despread energy for each particular multi-path component into a buffer (see blocks 524, 526 in figure 5).

Easton discloses all of the above subject matters but does not explicitly teaches a weighting element that weights the despread energy for a particular multi-path component using a channel estimate of the particular multi-path component. However, as shown in figure 3, Usuda teaches a weighting element that weights the despread signal for a particular multi-path component using a channel estimate of the particular multi-path component (see blocks 303, 306, and 307 in figure 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Usuda into the teaching of Easton in order to improve the

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reliability of the antenna weight for the data demodulation as well as to improve the communication quality and increase the radio channel capacity (column 3, lines 36-38 and lines 53-54).

(3) with regard to claim 8:

Easton further teaches a power control operable to power-down circuitry after the processing of all desired multi-path components and to power-up when the next buffer of sample data is ready to be processed (column 13, lines 45-59).

(4) with regard to claim 11:

Easton and Usuda further teach the accumulator that accumulates the despread energy for each particular multi-path component into a buffer selectively locates the despread energy into an output memory buffer (see figure 3 in Usuda reference).

(5) with regard to claim 12:

Easton further teaches circuitry to perform searches for multi-path components by correlating against a timing hypothesis (see figures 6C and 7).

(6) with regard to claim 15:

As shown in figure 2, Easton further teaches means for tuning to a non-original RF frequency (see block 214 in figure 2);

means for buffering digital samples obtained while tuned at the non-original RF frequency (see block 224 in figure 2);

means for retuning the RF frequency to the original frequency (see block 214 in figure 2); and

means for performing searching and channel estimation via the random access of the digital samples stored in the first memory element (see block 224 in figure 2) while simultaneously operating on the digital samples of the original frequency (see blocks 214 and 224 in figure 2).

(7) with regard to claim 16:

Easton further teaches means for buffering digital samples obtained while tuned at the non-original RF frequency maintains digital samples from the non-original RF frequency after retuning the RF frequency to the original frequency (see buffer 224 in figure 2).

(8) with regard to claim 17:

Easton further teaches means for processing a plurality of sets of digital samples from a plurality of distinct receiver RF chains (see figure 6A, note that this is a multipath system).

(9) with regard to claim 18:

Easton further teaches means for processing multi-path components corresponding to transmit diversity (see column 17, lines 24-34).

(10) with regard to claim 19:

As shown in figure 3, Usuda teaches means for dynamically switching to optimal functionality based on channel estimates (see channel estimator 303 in figure 3).

(11) with regard to claim 20:

As shown in figures 2 and 5, Easton discloses a demodulator operable with spread spectrum signals in a multi-path communication environment, the demodulator comprising:

a despreader that obtains digital samples from a first memory buffer by randomly accessing the first memory buffer, whereby the despreader is adaptable to arbitrary sample rates and symbol times (column 12, lines 23-30);

an accumulator that accumulates the digital samples from the despreader into a second memory buffer (blocks 526, 524 in figure 5),

Easton discloses all of the above subject matters but is silent about a channel estimator that obtains digital sample information from the despreader and provides a channel estimate of a particular multi-path component. However, having a channel estimator that obtains digital sample information from the despreader and provides a channel estimate of a particular multi-path component is well known in the art as it is evident by Usuda (see block 303 in figure 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Usuda into the teaching of Easton in order to improve the reliability of the antenna weight for the data demodulation as well as to improve the communication quality and increase the radio channel capacity (column 3, lines 36-38 and lines 53-54).

(11) with regard to claim 21:

Usuda further discloses an algorithm used to accumulate the digital samples into the memory buffer is selected dynamically via the channel estimate (see figure 3).

(12) with regard to claim 22:

Easton further teaches the digital samples are randomly accessible from the first memory buffer (see block 224 in figure 5).

(13) with regard to claim 23:

Easton further teaches a feedback in which data is read from the second memory buffer and used in the accumulation of the digital samples from the despreader into the second memory buffer (see figure 5, blocks 522, 524, and 234).

(14) with regard to claim 24:

Easton further teaches the accumulated digital samples comprise partially processed symbols (blocks 524, 234 in figure 5).

(15) with regard to claim 25:

Easton further discloses a power controller configured to toggle between an off state and an on state (column 13, lines 45-59).

(16) with regard to claim 28:

Easton further teaches the digital samples obtained from the first memory buffer include signals communicated in a multiple transmit, multiple receive antenna scheme (see block 224 in figure 5).

(17) with regard to claim 29:

Easton further teaches the accumulator that accumulates the digital samples from the despreader selectively locates the digital samples into the second memory buffer (see blocks 524 and 234 in figure 5).

7. Claims 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton et al. (US 6,985,516) in view of Usuda et al. (US 6,853,839) and further in view of Sriram et al. (US 2002/0176489).

(1) with regard to claim 9:

Easton and Usuda disclose all of the subject matters in claim 7 above except for there are three physically separate buffers such that at any given time, one of the three physically separate buffers is receiving data, and two of the three physically separate buffers comprise a logical buffer for random access by a correlator.

However, Sriram discloses there are three physically separate buffers (see figure 7) such that at any given time, one of the three physically separate buffers is receiving data, and two of the three physically separate buffers comprise a logical buffer for random access by a correlator (page 2, paragraph [0020]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Sriram into the teaching of Easton and Usuda in order to

present a significant advancement in the art of correlation processing (page 5, paragraph [0050]).

(2) with regard to claim 10:

Easton and Usuda disclose all of the subject matters in claim 7 above except for there are five physically separate buffers such that at any given time, two of the five physically separate buffers comprise a logically addressable space that is receiving data, and the other three of the five physically separate buffers comprise a logically addressable space for random access by a correlator.

However, Sriram discloses there are five physically separate buffers (see group of buffers in figure 7) such that at any given time, two of the five physically separate buffers comprise a logically addressable space that is receiving data, and the other three of the five physically separate buffers comprise a logically addressable space for random access by a correlator (page 2, paragraph [0020]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Sriram into the teaching of Easton and Usuda in order to present a significant advancement in the art of correlation processing (page 5, paragraph [0050]).

8. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton et al. (US 6,985,516) in view of Usuda et al. (US 6,853,839) and further in view of Wang (US 2002/009417).

(1) with regard to claim 13:

Easton and Usuda disclose all of the subject matters in claim 7 above except for separate sets of physical buffers for even and odd digital samples followed by a permutation block capable of mapping to one set of the separate sets of physical buffers to the searching element and one set of the separate sets of physical buffers to the demodulation element, whereby the permutation block manages contention between the searching element and the demodulation element for data in a same memory block.

Wang teaches separate sets of physical buffers for even and odd digital samples and provides the samples to a demodulator and a searcher (figure 4; page 2, paragraph [0017]; page 3, paragraphs [0026] and [0028]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Wang into the teaching of Easton and Usuda in order to improve the searcher speed and thus the finger update rate to improve wireless communication receiver performance (pages 1, 2, paragraph [0009]).

(2) with regard to claim 14:

Wang further discloses the permutation block is selected by providing correct timing of digital samples to the demodulator (block 206 in figure 4), and by providing the searching element with the other set of digital samples (block 208 in figure 4).

9. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton et al. (US 6,985,516) in view of Usuda et al. (US 6,853,839) and further in view of Joshi et al. (US 6,795,489).

(1) with regard to claim 26:

Easton and Usuda disclose all of the subject matters in claim 20 above except for the digital samples obtained from the first memory buffer include a burst-pilot signal that is time-division multiplexed, wherein the burst-pilot signal includes information relating to a cellular channel used to determine the channel estimate. However, including a burst-pilot signal that is time-division multiplexed and the burst-pilot signal includes information relating to a cellular channel used to determine the channel estimate is well known in the art as it is evident by Joshi (column 4, lines 54-67; column 5, lines 60-column 6, lines 1-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Joshi into the teaching of Easton and Usuda in order to provide accurate channel estimation as well as to improve the efficiency of the communication system.

(2) with regard to claim 27:

Easton and Usuda disclose all of the subject matters in claim 20 above except for the digital samples obtained from the first memory buffer include a continuous-pilot signal, wherein the continuous-pilot signal includes information relating to a cellular channel used to determine the channel estimate. However, including a continuous-pilot signal that includes information relating to a cellular channel used to determine the channel estimate is well known in the art as it is evident by Joshi (column 1, lines 27-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Joshi into the teaching of Easton and Usuda in order to provide accurate channel estimation as well as to improve the efficiency of the communication system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julia P. Tu whose telephone number is 571-270-1087. The examiner can normally be reached on 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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04/11/2007


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